IN THE CLAIMS

Please amend claims 43 and 47 as follows below.

Please cancel claim 48 without prejudice.

The following is a listing of claims that replaces all prior versions, and listings, of claims in the application:

Listing of Marked Up Claims:

1-22. (Cancelled).

23. (Previously Presented) A bipolar transistor, comprising:

a substrate to provide a collector region;

a base region having an intrinsic base region and an extrinsic base region, each of the intrinsic base region and the extrinsic base region having a mono-crystalline portion over a mono-crystalline portion of the substrate; and

an emitter structure over the intrinsic base region;

wherein the extrinsic base region is raised relative to the intrinsic base region;

wherein the extrinsic base region has a thickness *x* and the intrinsic base region has a thickness *y*, and wherein *x* is greater than *y*.

24. (Previously Presented) The bipolar transistor of claim 23, wherein

the emitter structure includes

a polysilicon emitter having a first portion with a width *a*, a second portion with a width *b*, and a third portion with a width *c*;

wherein *c* is greater than *b* which is greater than *a*; and

wherein the first portion defines an emitter base junction, and wherein the third portion defines an emitter contact region.

25. (Previously Presented) The bipolar transistor of claim 24, wherein

the emitter structure further includes a nitride spacer directly adjacent to the polysilicon emitter.

26. (Original) The bipolar transistor of claim 23, wherein

the extrinsic base region comprises:

a first epitaxial layer; and

a second epitaxial layer on the first epitaxial layer.

27. (Previously Presented) The bipolar transistor of claim 26, wherein

the first epitaxial layer is a SiGe epitaxial layer and the second epitaxial layer is a heavily p-type doped Si or SiGe epitaxial layer.

28. (Previously Presented) The bipolar transistor of claim 23, wherein

the bipolar transistor is an npn transistor.

29. (Previously Presented) A bipolar transistor, comprising:

a substrate having a collector region, the collector region being a collector terminal;

a first epitaxial silicon layer having a mono-crystalline portion on a mono-crystalline portion of the substrate;

an emitter stack on the first epitaxial silicon layer, the emitter stack being an emitter terminal;

a second epitaxial silicon layer having a mono-crystalline portion on the mono-crystalline portion of the first epitaxial silicon layer located outside the emitter stack;

wherein a region of the first epitaxial silicon layer located under the emitter stack is an intrinsic base region and a region of the second epitaxial silicon layer on portions of the first epitaxial silicon layer located outside the emitter stack being a raised extrinsic base region;

wherein the raised extrinsic base region has a thickness greater than a thickness of the intrinsic base region; and

wherein the intrinsic base region and the raised extrinsic base region provide a base terminal of the bipolar transistor with lower resistivity.

30. (Previously Presented) The bipolar transistor of claim 29, wherein

the first epitaxial layer is a p-type Si, SiGe or SiGe:C epitaxial layer and

the second epitaxial layer is a selectively deposited heavily p-type doped Si epitaxial layer or a selectively deposited heavily p-type doped SiGe epitaxial layer.

31. (Previously Presented) The bipolar transistor of claim 29, wherein

the emitter stack includes

a nitride layer having an emitter window, and

a polysilicon emitter within the emitter window.

32. (Previously Presented) The bipolar transistor of claim 29, wherein

the bipolar transistor is a Si, SiGe or SiGe:C npn bipolar transistor.

33. (Previously Presented) A bipolar transistor having a base, a collector, and an emitter, the bipolar transistor comprising:

a substrate with a collector region;

a base region coupled to the substrate, the base region having an intrinsic base region and an extrinsic base region, each of the intrinsic base region and the extrinsic base region having a mono-crystalline portion over a mono-crystalline portion of the substrate;

a polysilicon emitter structure coupled to the intrinsic base region; and

wherein the extrinsic base region has a thickness X and the intrinsic base region has a thickness *y*, and wherein *X* is greater than *Y*.

34. (Previously Presented) The bipolar transistor of claim 33, wherein

the extrinsic base region is raised relative to the intrinsic base region.

35. (Previously Presented) The bipolar transistor of claim 33, wherein

the polysilicon emitter structure has a first portion providing an emitter base junction, a second portion providing conduction, and a third portion providing an emitter contact region.

36. (Previously Presented) The bipolar transistor of claim 35, wherein

the first portion of the polysilicon emitter structure has a width *A*,

the second portion of the polysilicon emitter structure has a width B differing from A,

the third portion of the polysilicon emitter structure has a width C differing from A and C.

37. (Previously Presented) The bipolar transistor of claim 36, wherein

the width C is greater than the width B which is greater than the width A.

38. (Previously Presented) The bipolar transistor of claim 23, wherein
the extrinsic base region further has a poly-crystalline portion over an oxide layer of the substrate.

39. (Previously Presented) The bipolar transistor of claim 23, further comprising:
a silicide layer on a top surface of the extrinsic base region to lower a contact resistance.

40. (Previously Presented) The bipolar transistor of claim 39, wherein
the silicide layer is a refractory metal silicide layer of $CoSi_2$ or $TiSi_2$.

41. (Previously Presented) The bipolar transistor of claim 29, wherein
the first epitaxial layer further has a poly-crystalline portion on an oxide layer of the substrate, and
the second epitaxial layer further has a has a poly-crystalline portion on the poly-crystalline portion of the first epitaxial layer.

42. (Previously Presented) The bipolar transistor of claim 29, further comprising:

a silicide layer on a top surface of the second epitaxial silicon layer to lower a contact resistance.

43. (Currently Amended) The bipolar transistor of claim [[40]] 42, wherein
the silicide layer is a refractory metal silicide layer of $CoSi_2$ or $TiSi_2$.

44. (Previously Presented) The bipolar transistor of claim 33, wherein
the extrinsic base region further has a poly-crystalline portion over an oxide layer of the substrate.

45. (Previously Presented) The bipolar transistor of claim 33, further comprising:
a silicide layer on a top surface of the extrinsic base region to lower a contact resistance.

46. (Previously Presented) The bipolar transistor of claim 45, wherein
the silicide layer is a refractory metal silicide layer of $CoSi_2$ or $TiSi_2$.

47. (Currently Amended) A bipolar transistor, comprising:
a substrate having a mono-crystalline portion and an oxide portion, the substrate to provide a collector region;
a plurality of epitaxial layers over the substrate, each of the plurality of epitaxial layers having a mono-

crystalline portion over the mono-crystalline portion of the substrate and a poly-crystalline portion over the oxide portion of the substrate; and

a polysilicon emitter on the mono-crystalline portion of a first epitaxial layer of the plurality of epitaxial layers;

wherein the plurality of epitaxial layers to provide a raised extrinsic base located outside the polysilicon emitter, the mono-crystalline portion of the first epitaxial layer under the polysilicon emitter to provide an intrinsic base, and the raised extrinsic base is thicker than the intrinsic base.

48. (Cancelled)

49. (Previously Presented) The bipolar transistor of claim 47, wherein

at least a second epitaxial layer of the plurality of epitaxial layers is coupled to the first epitaxial layer to provide the raised extrinsic base.

50. (Previously Presented) The bipolar transistor of claim 49, wherein

the first epitaxial layer is a SiGe epitaxial layer and

the at least second epitaxial layer is a heavily p-type doped Si or SiGe epitaxial layer.

51. (Previously Presented) The bipolar transistor of claim 47, further comprising:

a silicide layer on a top surface of the raised extrinsic base to lower a contact resistance.

52. (Previously Presented) The bipolar transistor of claim 51, wherein
the silicide layer is a refractory metal silicide layer of $CoSi_2$ or $TiSi_2$.

53. (Previously Presented) The bipolar transistor of claim 47, wherein
the bipolar transistor is an npn transistor.

54. (Previously Presented) The bipolar transistor of claim 53, wherein
the npn transistor is a Si, SiGe or SiGe:C npn bipolar transistor.